FIG.1

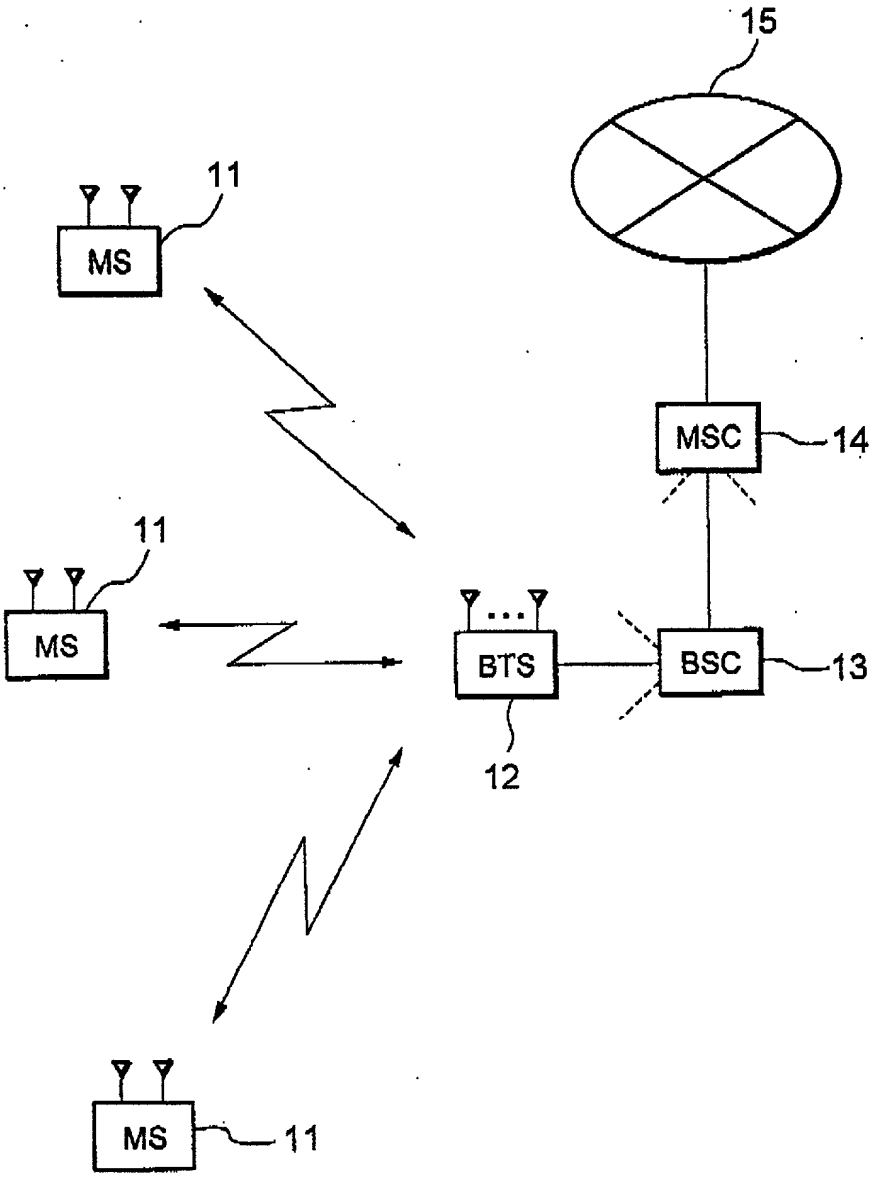


FIG.2

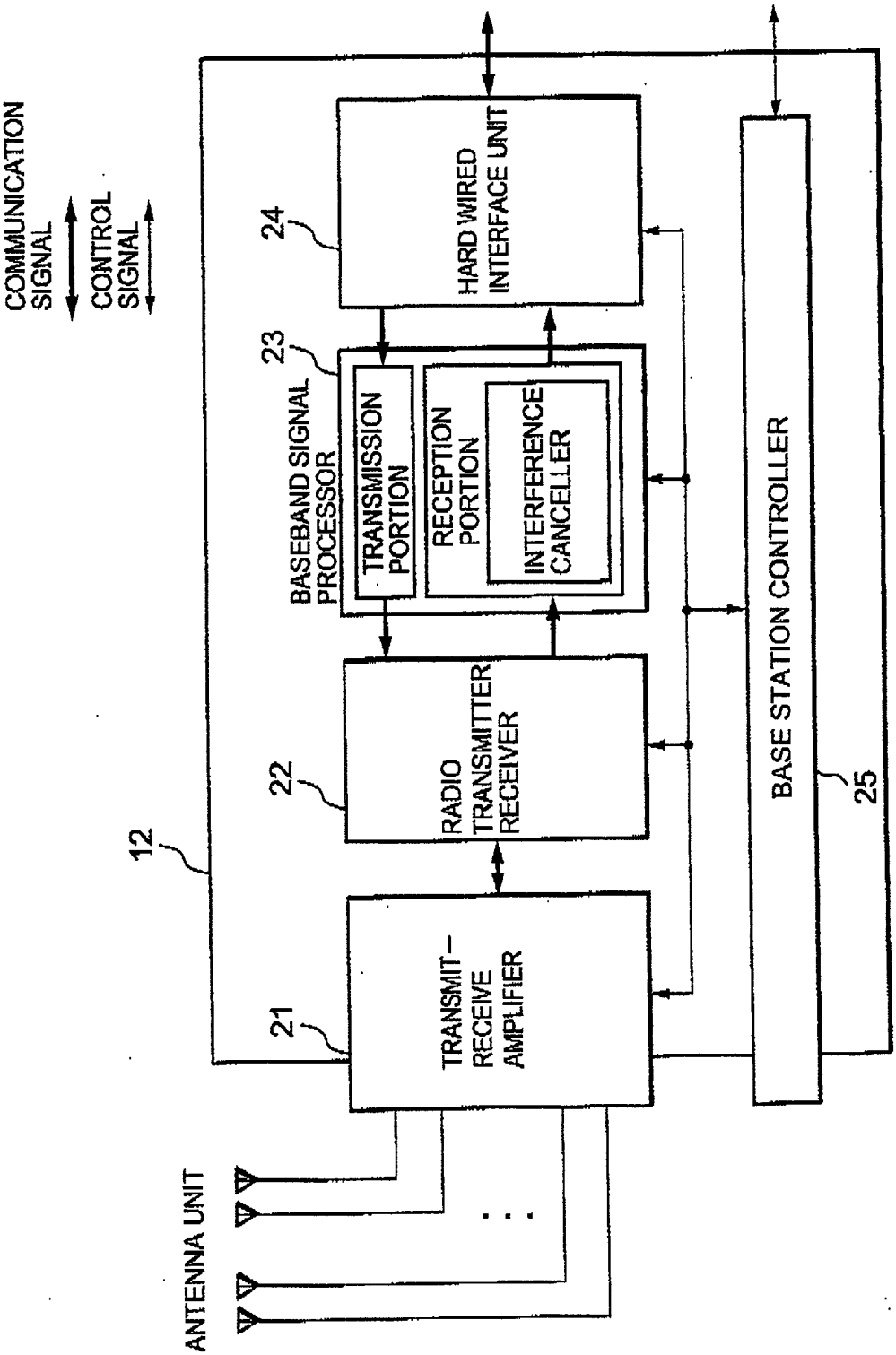

COMMUNICATION SIGNAL
CONTROL SIGNAL
12
ANTENNA UNIT
21
TRANSMIT–RECEIVE AMPLIFIER
22
RADIO TRANSMITTER RECEIVER
23
BASEBAND SIGNAL PROCESSOR
TRANSMISSION PORTION
RECEPTION PORTION
INTERFERENCE CANCELLER
24
HARD WIRED INTERFACE UNIT
25
BASE STATION CONTROLLER

FIG.3

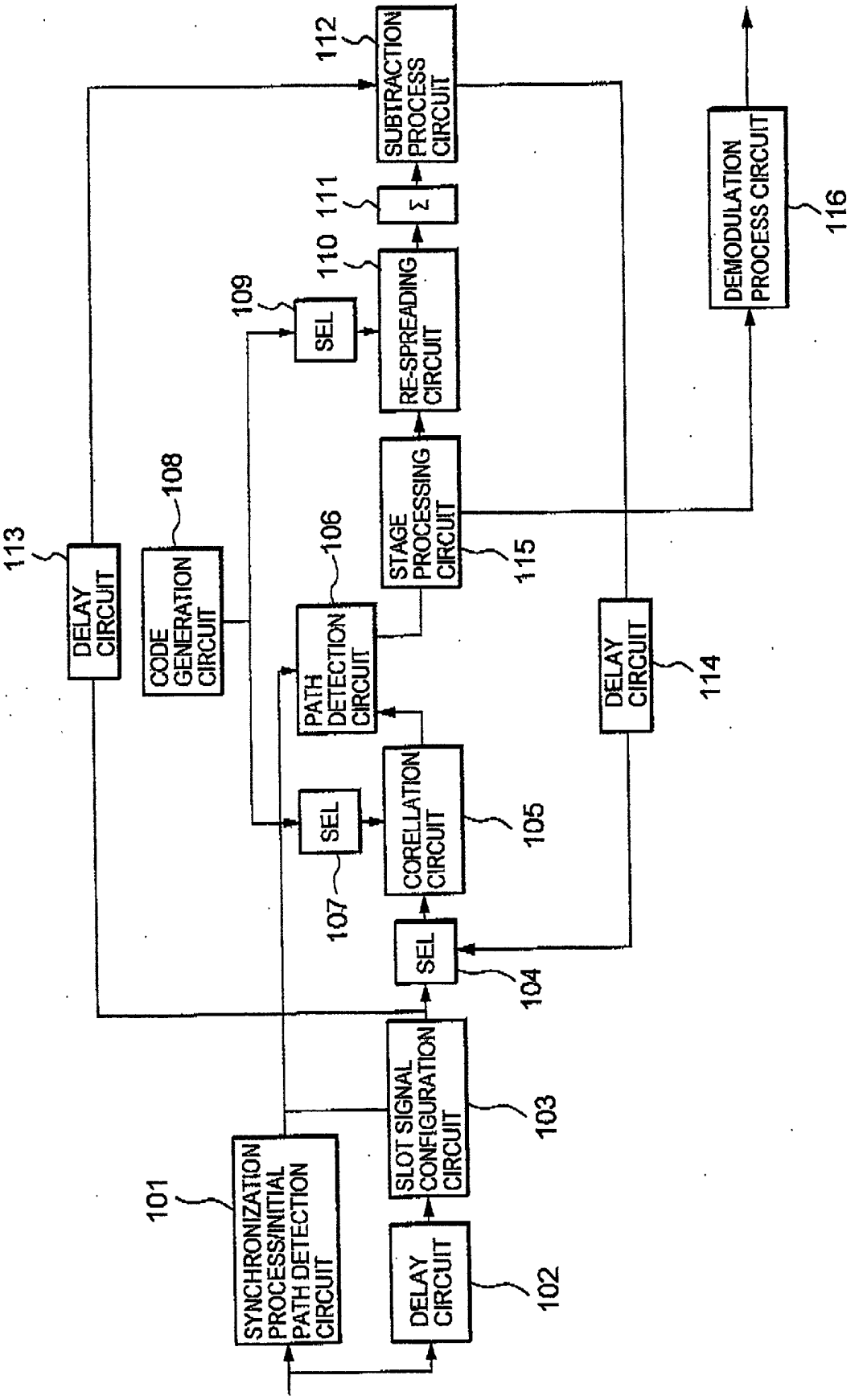
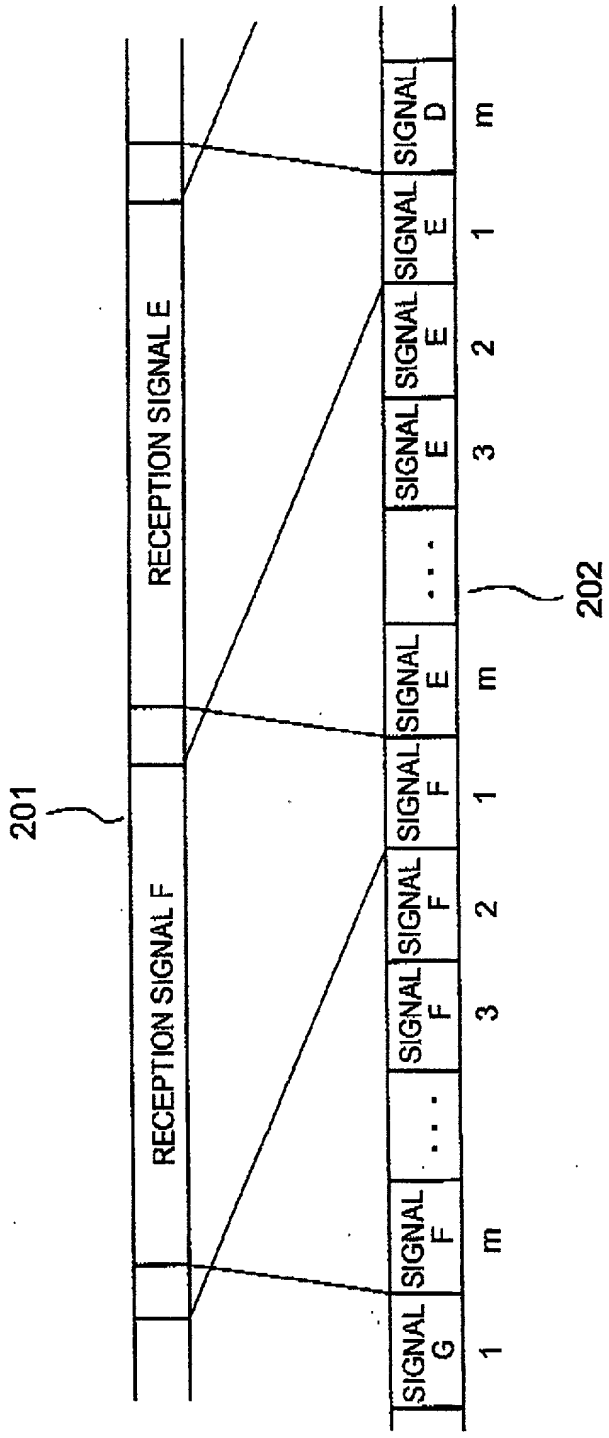

SYNCHRONIZATION PROCESS/INITIAL PATH DETECTION CIRCUIT
101
DELAY CIRCUIT
102
SLOT SIGNAL CONFIGURATION CIRCUIT
103
SEL
104
CORELLATION CIRCUIT
105
PATH DETECTION CIRCUIT
106
SEL
107
CODE GENERATION CIRCUIT
108
SEL
109
RE-SPREADING CIRCUIT
110
Σ
111
SUBTRACTION PROCESS CIRCUIT
112
DELAY CIRCUIT
113
DELAY CIRCUIT
114
STAGE PROCESSING CIRCUIT
115
DEMODULATION PROCESS CIRCUIT
116

FIG.4


201
RECEPTION SIGNAL F
RECEPTION SIGNAL E
SIGNAL G
SIGNAL F
SIGNAL F
SIGNAL F
SIGNAL F
SIGNAL F
SIGNAL E
SIGNAL E
SIGNAL E
SIGNAL E
SIGNAL D
1
m
3
2
1
m
3
2
1
m
202

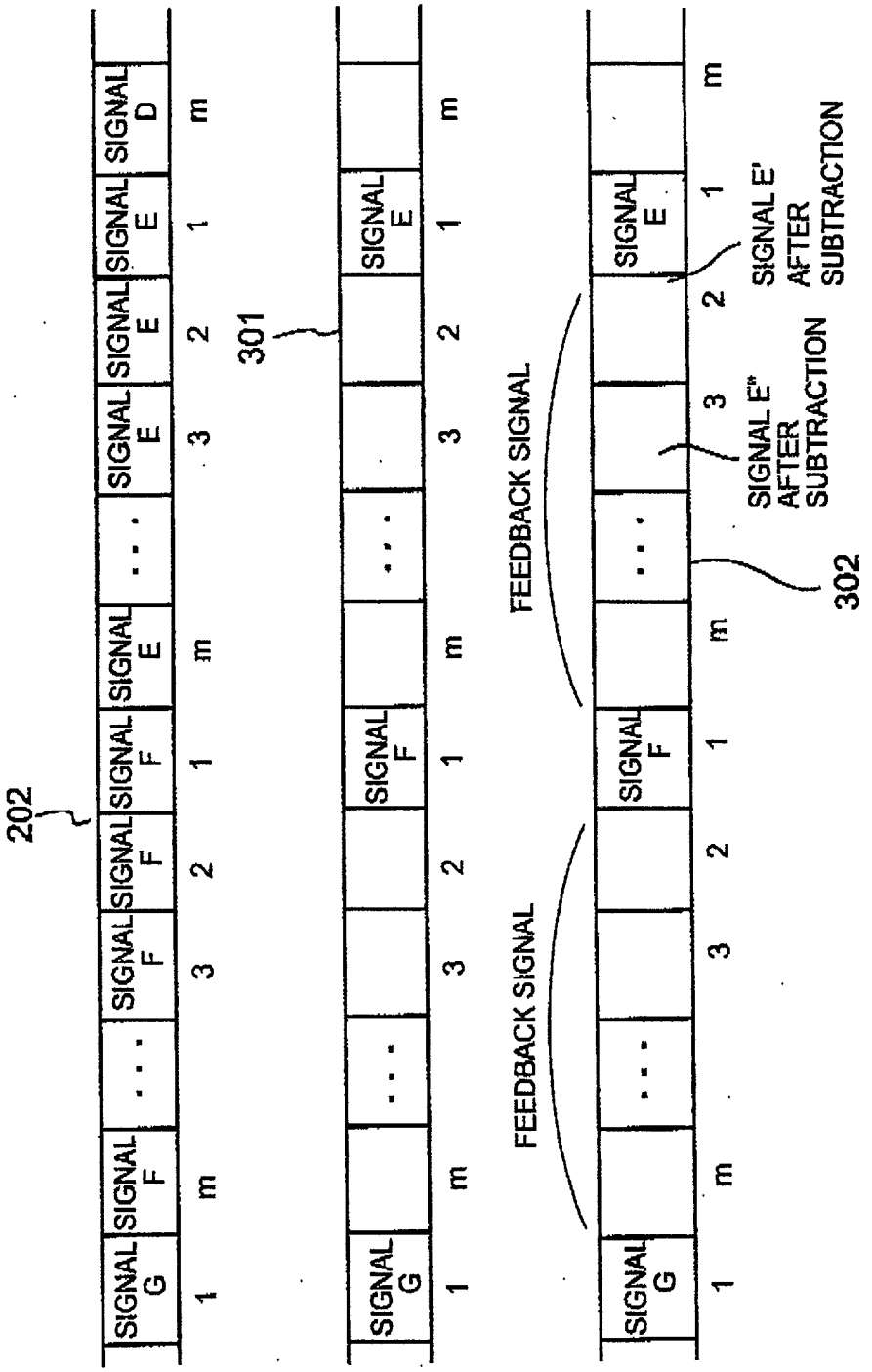


FIG.5A

FIG.5B

FIG.5C

FIG.6A

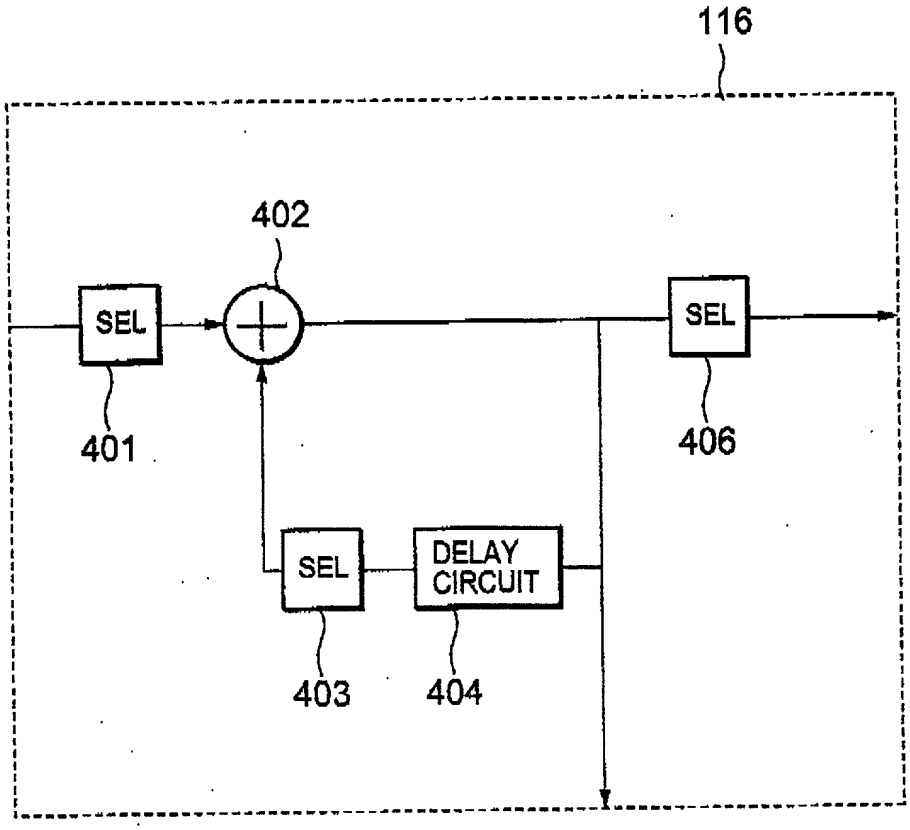

116
402
SEL
401
SEL
406
SEL
403
DELAY CIRCUIT
404

FIG.6B

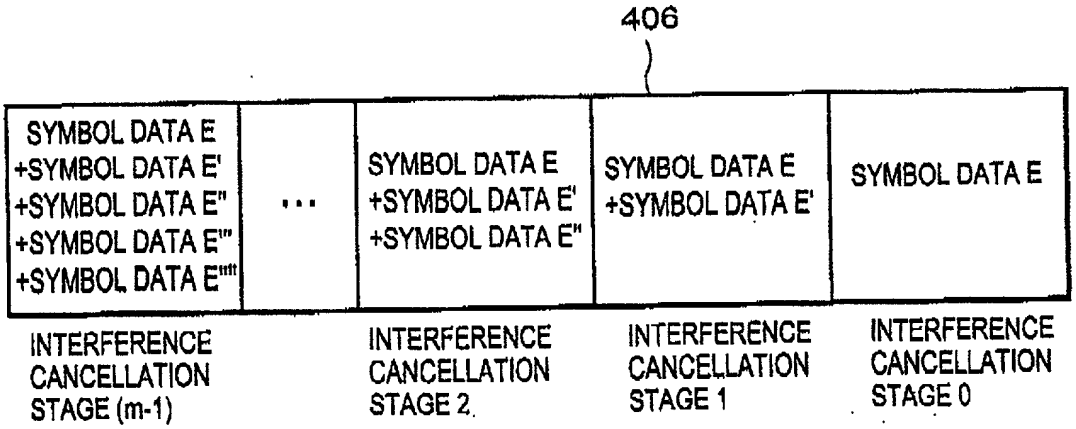

406
SYMBOL DATA E +SYMBOL DATA E' +SYMBOL DATA E" +SYMBOL DATA E'" +SYMBOL DATA E""
...
SYMBOL DATA E +SYMBOL DATA E' +SYMBOL DATA E"
SYMBOL DATA E +SYMBOL DATA E'
SYMBOL DATA E
INTERFERENCE CANCELLATION STAGE (m-1)
INTERFERENCE CANCELLATION STAGE 2
INTERFERENCE CANCELLATION STAGE 1
INTERFERENCE CANCELLATION STAGE 0

FIG.7

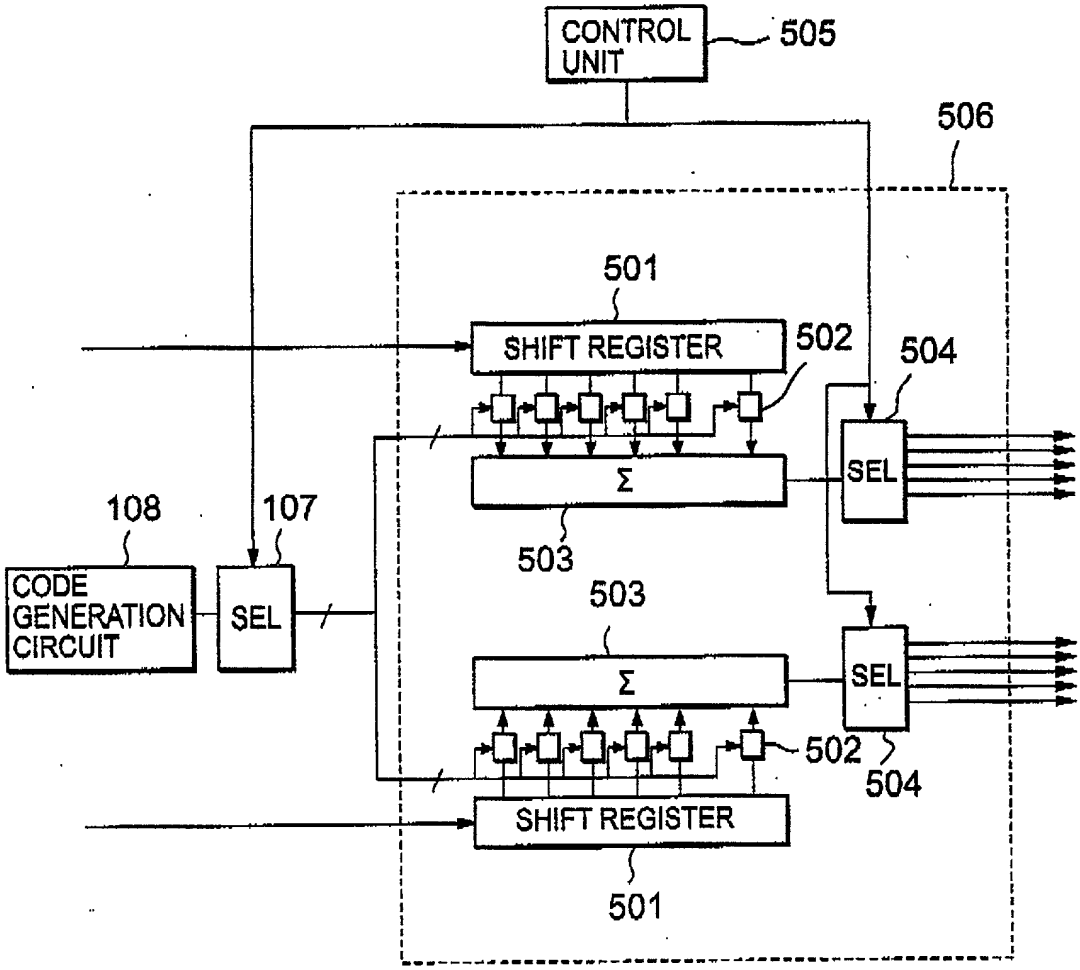

CONTROL UNIT
505
506
501
SHIFT REGISTER
502
504
Σ
SEL
503
108
107
CODE GENERATION CIRCUIT
SEL
503
Σ
SEL
502
504
SHIFT REGISTER
501

FIG.8

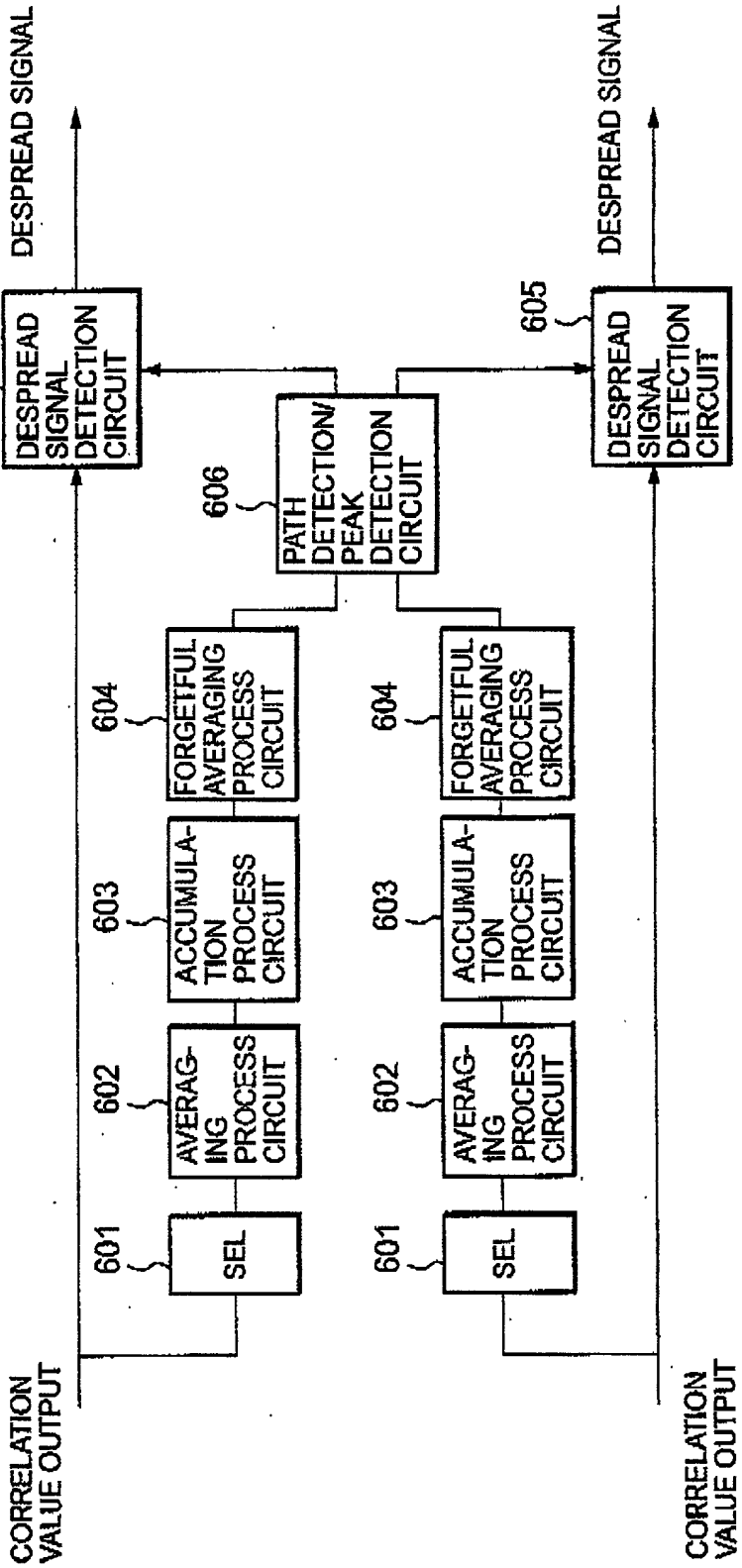
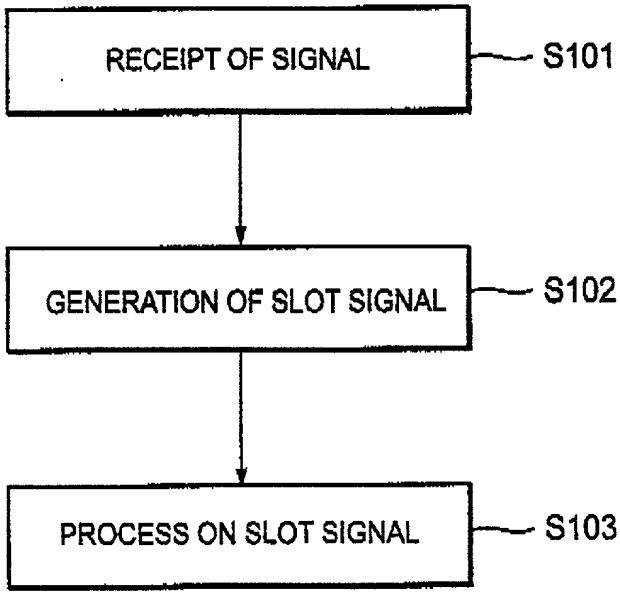

DESPREAD SIGNAL
605
DESPREAD SIGNAL DETECTION CIRCUIT
606
PATH DETECTION/ PEAK DETECTION CIRCUIT
604
FORGETFUL AVERAGING PROCESS CIRCUIT
603
ACCUMULATION PROCESS CIRCUIT
602
AVERAGING PROCESS CIRCUIT
601
SEL
CORRELATION VALUE OUTPUT
DESPREAD SIGNAL
605
DESPREAD SIGNAL DETECTION CIRCUIT
604
FORGETFUL AVERAGING PROCESS CIRCUIT
603
ACCUMULATION PROCESS CIRCUIT
602
AVERAGING PROCESS CIRCUIT
601
SEL
CORRELATION VALUE OUTPUT

FIG.9


RECEIPT OF SIGNAL
S101
GENERATION OF SLOT SIGNAL
S102
PROCESS ON SLOT SIGNAL
S103